A Term Paper Report on

SIMULATION AND IMPLEMENTION OF VEDIC MULTIPLIER USING VHDL

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<u>CERTIFICATE</u>

This is to certify that this is a bonafide report of term paper titled "**SIMULATION AND IMPLENTATION OF VEDIC MULTIPLIER USING VHDL**" *being submitted by D.RAMAYAMINI(Y11EC818), D.V.RAMA VATHI(Y11EC819),G.RAMYA SREE(L12EC929), D.RAVI KRISHNA(Y11EC821) towards the paper with code EC453 during IV/IV B.Tech I semester in the academic year 2014-2015.*

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABSTRACT:

The main aim of the project is to improve the speed of the complex multiplier by using Vedic mathematics. This 'Vedic Mathematics' is the name given to the ancient system of mathematics or, to be precise, a unique technique of calculations based on simple rules and principles with which any mathematical problem can done with the help of arithmetic, algebra, geometry or trigonometry can be solved. Traditionally complex multiplier provides less speed only, because it does not use Vedic Mathematics concept. By using 'Vedic Mathematics' concept we can skip carry propagation delay. The system is based on 16Vedic sutras, in which we are using one kind of Vedic sutra describing natural ways of solving a whole range of mathematical problems .The main design features of the proposed system are the reconfigurability and flexibility. Architecture of Vedic multiplier based on specification is designed here for following criteria Increase the Speed of the system. To acquire good efficiency of the system Reduce the time delay as well as path delay in the multiplier The combinational path delay of Vedic multiplier obtained after compared with normal multipliers and found that the proposed Vedic multiplier.

In a typical processor, Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and Processing time than addition and subtraction. In fact, 8.72% of all the instruction in typical processing units is multipliers. In computers, a typical central processing unit devotes a considerable amount of processing time in implementing arithmetic operations, particularly multiplication operations .In this project , the comparative study of different multipliers is done for low power requirement and high speed, also gives information of "Urdhva Tiryakbhyam" algorithm of Ancient Indian Vedic Mathematics which is utilized for multiplication to improve the speed, area parameters of multipliers. Vedic Mathematics also suggests one more formulae for multiplication. "Nikhilam Sutra" which can increase the speed of

multiplier by reducing the number of iterations. Which increase the speed of the multiplier as well as processor or system.

CHAPTER1

INTRODUCTION

1.1.INTRODUCTION:

Multiplication methods are extensively discussed in Vedic mathematics. Various tricks and short cuts are suggested by Vedic Mathematics to optimize the process. These methods are based on concept of 1 Multiplication using deficits and excess 2 changing the base to simplify the operation. Various methods of multiplication proposed in Vedic Mathematics.

a) UrdhvaTiryagBhyam - vertically and crosswise

b) Nikhilam navatashcharamam Dashatah: All from nine and last from ten

1.1.1.Urdhva Tiryakbhyam Sutra

The multiplier is based on an algorithm UrdhvaTiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. Power dissipation which results in higher device operating temperatures. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient.

1.1.2.Nikhilam Sutra

Nikhilam Sutra literally means "all from 9 and last from 10". Although it is applicable to all cases of multiplication, it is more efficient when the numbers involved are large. Since it finds out the compliment of the large number from its nearest base to perform the multiplication operation on it, larger is the original number, lesser the complexity of the multiplication. For example, we first

illustrate this Sutra by considering the multiplication of two decimal numbers (96 * 93) where the chosen base is 100 which is nearest to and greater than both these two numbers.

1.2. VHDL:

It is acronym of VHSIC Hardware Description Language. VHSIC stands for Very High Speed Integrated Circuits. It is a hardware description language used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits. VHDL can also be used as a general purpose parallel programming language.

When a VHDL model is translated into the "gates and wires" that are mapped onto a programmable logic devices. It is the actual hardware being configured, rather than the VHDL code being "executed" as if on some form of a processor chip.

1.3.Comparison between normal multiplier and Vedic Multiplier:

Aspect	Normal multiplier	Vedic Multiplier
Speed	They possess comparatively less speed.	Vedic Multipliers possess high speed comparatively.
Efficiency	Less efficient.	More efficient.
Time delay	More carry generation and propagation leads to more delay of time.	Due to less generation of carry, time delay is reduced in case of Vedic Multiplier.
Power required	To work with normal multiplier and its implementation requires more power.	Vedic Multipliers requires comparatively less power.

1.4. LIST OF 16 SUTRAS OF VEDIC MATHEMATICS:

1) (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.

2) Chalana-Kalanabyham – Differences and Similarities.

3) Ekadhikina Purvena – By one more than the previous One.

4) Ekanyunena Purvena – By one less than the previous one.

5) Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.

6) Gunitasamuchyah – The product of the sum is equal to the sum of the product.

7) Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.

8) Paraavartya Yojayet – Transpose and adjust.

9) Puranapuranabyham – By the completion or non completion.

10) Sankalana- vyavakalanabhyam – By addition and by subtraction.

11) Shesanyankena Charamena – The remainders by the last digit.

12) Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.

13) Sopaantyadvayamantyam – The ultimate and twice the penultimate.

14) Urdhva-tiryakbhyam – Vertically and crosswise.

15) Vyashtisamanstih – Part and Whole.

16) Yaavadunam – Whatever the extent of its deficiency.

CHAPTER 2

IMPLEMENTATION OF 2X2 VEDIC MULTIPLIER

2.1.Implementation of 2x2 bit Vedic Multiplier

The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay, which is the primary motivation behind this work.

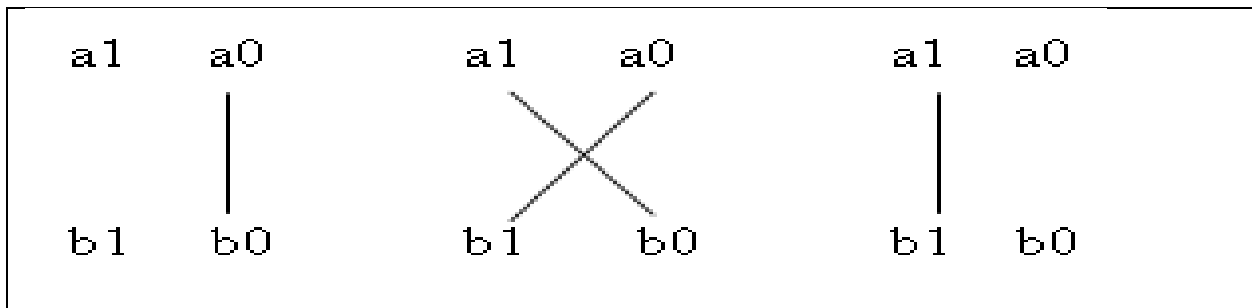Here we are implementing the Vedic Multiplication technique for two 2-digits numbers.

Fig1: The Vedic Multiplication Method for two 2-bit Binary Numbers The 2X2 Vedic multiplier module is implemented

Representing the multiplication operation of   a1 a0

b1 b0

_____

_____

In fig 2, The method is explained below for two, 2 bit numbers A and B where $A = a1a0$ and $B = b1b0$ as shown in Fig. 2.

Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next block higher bit

of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise).
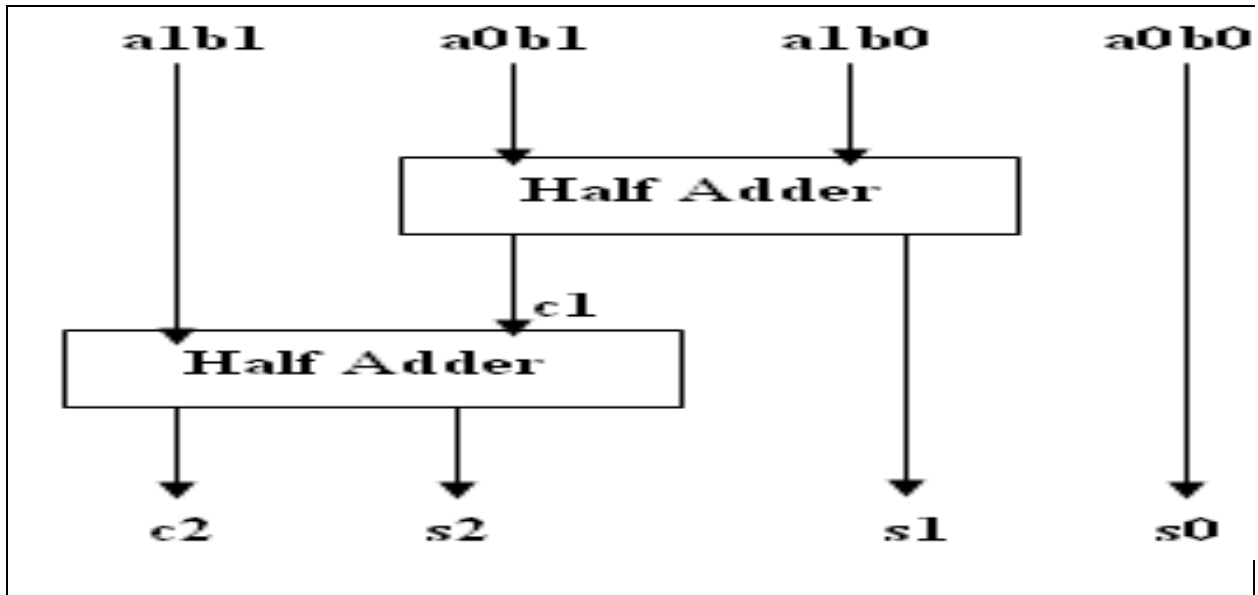
2.2.Block Diagram representation

Fig 2: Block Diagram of 2x2 bit Vedic Multiplier

The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

$$s0 = a0b0; \longrightarrow (1)$$

$$c1s1 = a1b0 + a0b1; \longrightarrow (2)$$

$$c2s2 = c1 + a1b1; \longrightarrow (3)$$

The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Fig. 3. It is found that the hardware architecture of 2x2 bit Vedic multiplier is same as the hardware architecture of 2x2 bit conventional Array Multiplier Hence it is concluded that multiplication of 2 bit binary numbers by Vedic method does not made significant effect in improvement of the multiplier's efficiency.

Very precisely we can state that the total delay is only 2-half adder delays, after final bit products are generated, which is very similar to Array multiplier.

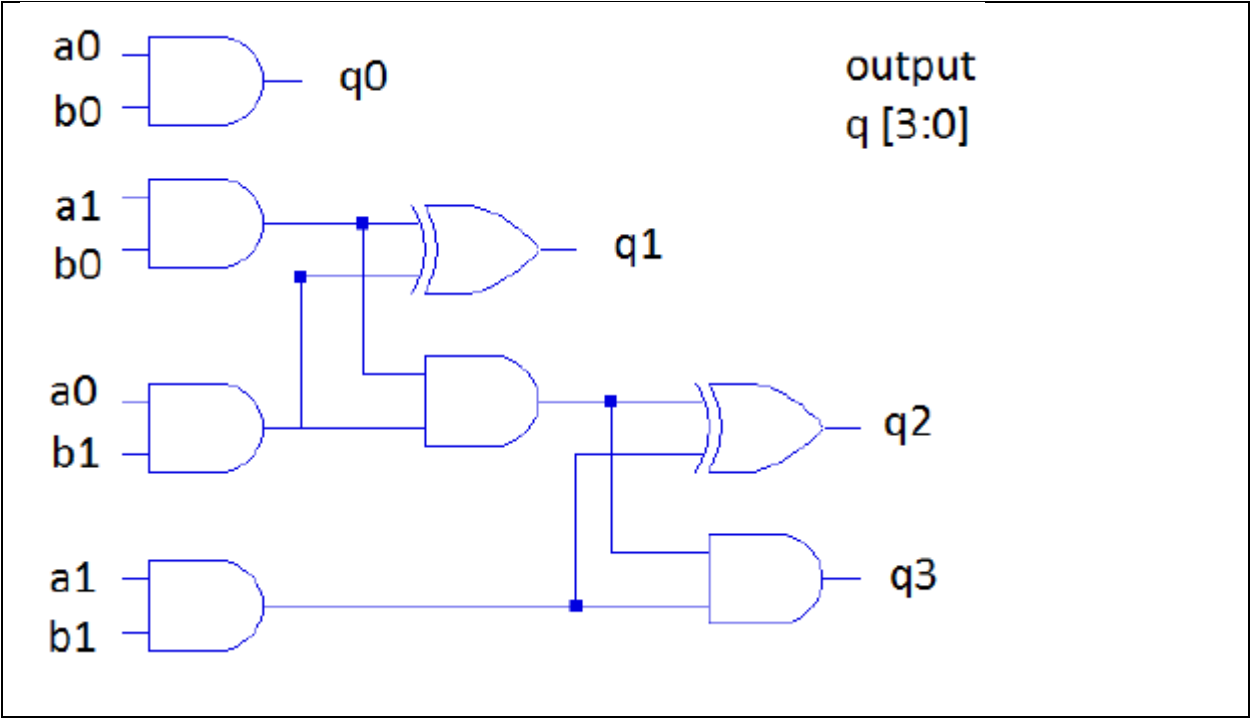## 2.3. Hard ware implementation

Fig 3: Hard ware implementation of 2X2 Vedic multiplier

The design starts first with Multiplier design, that is 2x2 bit multiplier as shown in fig 3.

Here, "Urdhva Tiryakbhyam Sutra" or "Vertically and Crosswise Algorithm" for multiplication has been effectively used to develop digital multiplier architecture. This algorithm is quite different from the traditional method of multiplication, which is to add and shift the partial products.

CHAPTER 3

IMPLEMENTATION OF 4x4 VEDIC MULTIPLIER

3.1.Line Diagram Implementation of 4x4 Vedic Multiplier

Here we are implementing the Vedic Multiplication technique for two 4-digits numbers.

Step1: **1 2 3 4**

1 2 3 4

step2: 1 2 3 4

1 2 3 4

Step3: 1 2 3 4

1 2 3 4

step4: 1 2 3 4

1 2 3 4

Step5: 1 2 3 4

1 2 3 4

step6: 1 2 3 4

1 2 3 4

Step7: 1 2 3 4

1 2 3 4

Fig4:line diagram for of 4x4 Vedic Multiplier

3.2. Hardware implementation of 4x4 Vedic multiplier

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules as discussed in Fig The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules as discussed in Fig4
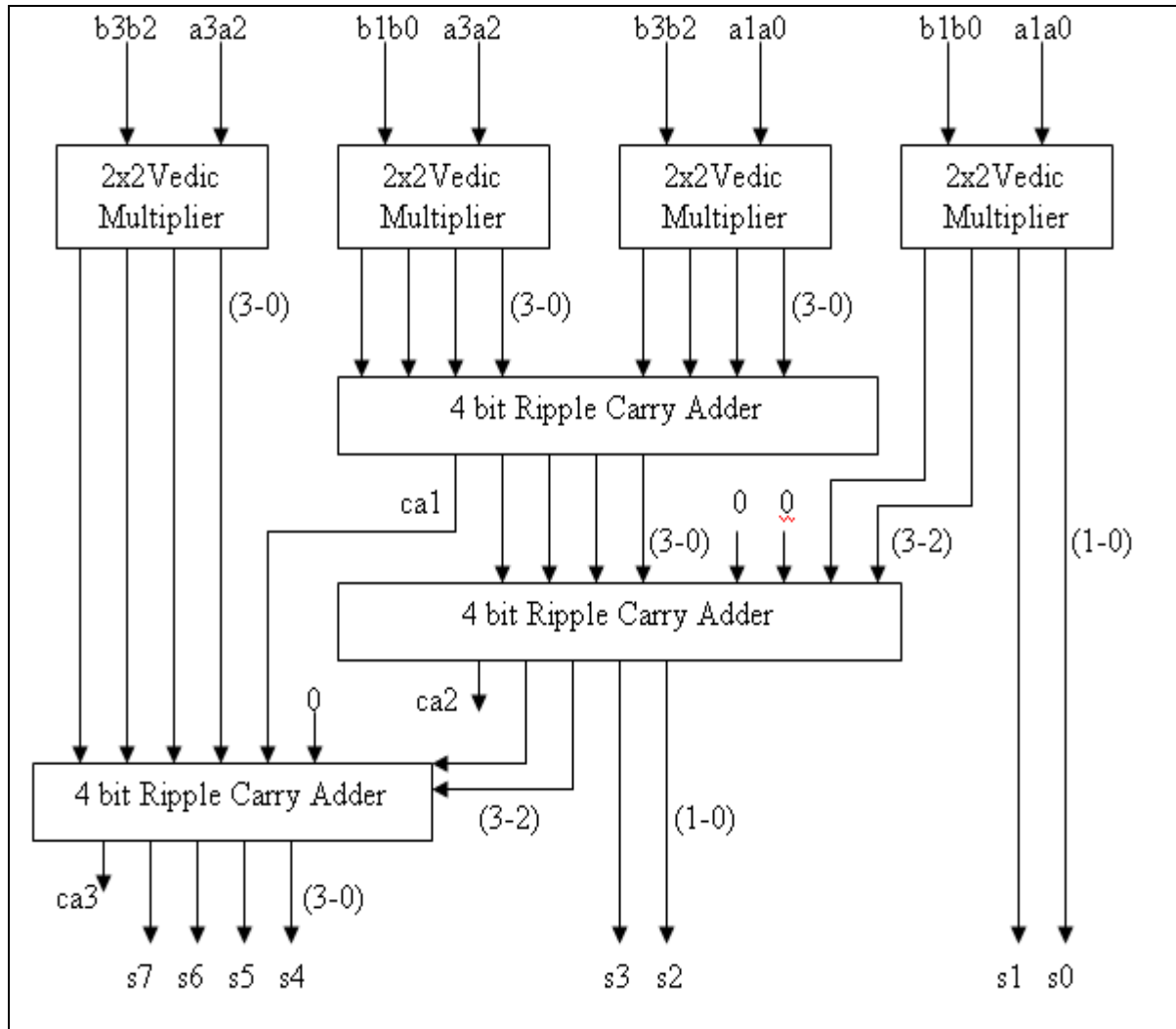

Fig5: Architechture of Urdhava Tiryakbhyam algorithm

Urdhava Tiryakbhyam integer multiplier is faster since all the partial products are computed concurrently. Considering a 16 bit Q15 multiplier, the product is also a Q15number which is 16 bits long. Firstly, if the MSB of input is 1then it is a negative number. Therefore 2's complement of the number is taken before proceeding with multiplication. Since the MSB denotes sign it is excluded and a '0' is placed in thisposition while multiplying. A Q15 format multiplier consists of four 8 x 8 Urdhava multipliers and the resulting product is 32 bits long as shown in fig. 4. But the product of a Q15 number is also a Q15 number which should be 16 bits long. Therefore the32 bit product is left shifted by 1 bit to remove the redundant sign bit and only the most significant 16 bits of this product are considered which constitute the final product. An xor operation is performed on the input sign bits to determine the sign of the result.

Let's analyze 4x4 multiplications, say A=A3 A2 A1A0and B=B3 B2 B1 B0. The output line for the multiplication result is –S7 S6 S5 S4 S3 S2 S1S0.Let's divide A and B into two parts, say A3 A2 & A1 A0 for A and B3 B2 & B1 B0 for B. Using the fundamental of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block, we can have the following structure for multiplication.

Which will produce a result bit (referred as s6s5s4s3s2s1s0) and carry (referred as cn)? It should be clearly noted that cn may be a multi-bit number.

Thus we get the following expressions

$$s0=a0b0 \qquad\qquad \ldots\ldots \quad (1)$$

$$s1r1=a1b0+a0b1 \qquad\qquad \ldots\ldots \quad (2)$$

$$s2r2=s1+a2b0+a1b1 + a0b2 \qquad \ldots\ldots \quad (3)$$

$$s3r3=s2+a3b0+a2b1 + a1b2 + a0b3 \qquad \ldots\ldots \quad (4)$$

$$s4r4=s3+a3b1+a2b2 + a1b3. \qquad \ldots\ldots \quad (5)$$

$$s5r5=s4+a3b2+a2b3 \qquad\qquad \ldots\ldots \quad (6)$$

$$s6r6=s5+a3b3 \qquad\qquad \ldots\ldots \quad (7)$$

To understand the concept, the Block diagram of 4x4 bit Vedic multiplier is shown in Fig. 4. To get final product (S7 S6 S5 S4 S3 S2 S1 S0), four 2x2 bit Vedic multiplier (Fig. 3) and three 4-bit Ripple-Carry (RC) Adders are required. The proposed Vedic multiplier can be used to reduce delay. Here, we proposed a new architecture, which is efficient in terms of speed. The arrangements of RC Adders shown in Fig. 4, helps us to reduce delay.

CHAPTER 4

ADVANTAGES AND APPLICATIONS

4.1.ADVATAGES:

Architecture of Vedic multiplier based on speed specification is designed here for following criteria

- Increase the Speed of the system

- To acquire good efficiency of the system

- Reduce the time delay as well as path delay in the multiplier

- Low power consumption

- The combinational path delay of Vedic multiplier obtained after compared with normal multipliers and found that the proposed Vedic multiplier.

4.1.1.SPEED:

Vedic multiplier is faster than Booth multiplier. As the number of bits increases from 8x8 bits to 16x16 bits, the timing delay is greatly reduced for Vedic multiplier as compared to other multipliers. Vedic multiplier has the greatest advantage as compared to other multipliers over gate delays and regularity of structures. Delay in Vedic multiplier for 16 x 16 bit number is 32 ns while the delay in Booth multiplier is 37ns. Thus this multiplier shows the highest speed among conventional multipliers. It has this advantage than others to prefer a best multiplier.

4.1.2. POWER:

Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. Minimizing power consumption for digital systems involves optimization at all levels of the design.

4.2.APPLICATIONS:

4.2.1.Microprocessors

4.2.1.1.Arithmetic & Logic Unit

Urdhava Tiryakbhyam is based on a novel concept through which all partial products are generated concurrently. Demonstrates a 4x4 binary multiplication using this method. The method can be generalized for any N x N bit multiplication. This is independent of the clock frequency of the processor because the partial products and their sums are Calculated in parallel. The net advantage is that it reduces the need of microprocessors to operate at increasingly higher clock frequencies. As the operating frequency of a processor increases the number of switching instances also increases. These results in more power consumption and also dissipation in the form of heat which results in higher device operating temperatures. Another advantage is its scalability. The processing power can easily be increased by increasing the input and output data bus Widths since it have a regular structure. Due to its regular structure, it can be easily layout in a silicon chip and also consumes optimum area. As the number of input bits Increase, gate delay and area increase very slowly as compared to other multipliers. Therefore Urdhava Tiryakbhyam multipliers time, space and power efficient.

4.2.1.2.ALU Design

Arithmetic and logic unit is at the heart of the digital circuits. Due to the complexity of the operations that needs to be performed nowadays by the processor, the demand for sharing the load by many special purpose processors is increased. Hence the speed, size and power efficiency of the ALU becomes important factors when designing an ALU. Use of Vedic mathematics for multiplication strikes a difference in actual process and hence reduces size and power. Urdhava Tiryakbhyam Sutra of Vedic mathematics to is used build a power efficient multiplier in the

coprocessor. The advantages of Vedic multipliers are increase in speed, decrease in delay, decrease in power consumption and decrease in area occupancy. It is stated that this Vedic coprocessor is more efficient than the conventional one.

4.2.2. Digital Image Processing:

4.2.2.1. Discrete Fourier Transform

There are many algorithms for finding DFT. But now a day's only VON-NEUMAN architectural implementation of classical method is found to be used in digital computers. Kulkarni analyses and compares the Implementation of Discrete Fourier Transform algorithm by existing and by Vedic mathematics techniques. He suggested that architectural level changes in the entire computation system to accommodate the Vedic Mathematics method increases the overall efficiency of DFT procedure.

4.2.2.2. FFT Implementation

A fast Fourier transform (FFT) is an algorithm to compute the discrete Fourier transform (DFT) and it's inverse. FFT is widely used in wireless communication imaging etc. Implementation of FFT requires large number of complex multiplications and complex additions, so to make this process rapid and simple it's necessary for a multiplier to be fast and power efficient. Vedic mathematics is an efficient method of multiplication.

FFT using "Vertically and crosswise" algorithm of Vedic mathematics and suggested that Vedic mathematics reduces the complex number multiplications and additions from N2 to N/2log2N and Nlog2N respectively and conclude that Vedic method is faster than the array multiplier architecture

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CHAPTER 5

CONCLUSION

5.1.CONCLUSION:

Vedic mathematics formulae can be used in various algorithms in different computer applications. Various parameters are considered for comparisons of different algorithms. It is concluded that the computer architectures designed using Vedic mathematics are proved to better the conventional architecture in terms of computation speed, power utilisation and silicon area. Various algorithm based on Vedic maths proved to have faster speed, less power and lesser area. The results obtained are also verified on various FPGAs. Further improvement can be done by reducing the delay caused by propagation of the carry generated from the intermediate products in the multipliers.

FUTURE SCOPE

Vedic mathematics deals with various topics of mathematics such as basic arithmetic, geometry, trigonometry, calculus etc. All these methods are very efficient as far as manual calculations are concerned. If all those methods effectively implementhardware, it will reduce the computational speed drastically. Therefore, it could be possible to implement a complete ALU using all these methods using Vedic mathematics methods.

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